SCOPE OF CLAIMS

1. A Fourier transform apparatus for performing discrete Fourier transform, characterized in the said Fourier transform apparatus comprises

transform means of a preceding stage including a number a of M-point radix 2 pipeline FFT circuits each having two parallel inputs/outputs, wherein $M(=2^m, m>=2)$ represents a maximum number of points for transform and a represents a divisor of said maximum transform point number M,

first data supply means for supplying input data to the transform means of said preceding stage in accordance with a first predetermined order,

transform means of a succeeding stage including a same number of M-point radix 2 pipeline FFT circuits as the transform means of said preceding stage, each of said FFT circuits having two parallel inputs/outputs,

second data supply means for supplying input data to the transform means of said succeeding stage in accordance with a second predetermined order, and

twiddle factor multiplication means including 2a complex multiplication circuits and storage means for storing twiddle factors, provided between the transform means of said preceding stage and the transform means of said succeeding stage for multiplication of twiddle factors.

2. A Fourier transform apparatus set forth in claim 1,

characterized in that said first data supply means includes a first memory circuit implemented in a two-bank structure, writing means for writing alternately and sequentially said input data on an M-by-M basis while changing over banks of said first memory circuit, and reading means for reading out simultaneously the data from corresponding positions of the two banks of said first memory circuit for supplying said data to the transform means of said preceding stage.

3. A Fourier transform apparatus set forth in claim 1,

characterized in that said first data supply means is comprised of first and second data permutating modules in two stages for permutating the data in a predetermined order, said first and second data permutating modules being composed of second and third memory circuits for storing data, a read or write address generating circuit conforming to predetermined logics of said second and third memory circuits, respectively, and corner turners for permutating data read out from said second and third memory circuits, respectively, and

that said second data supply means is comprised of third data permutating module, said third data permutating module being composed of a fourth memory circuit for storing data, a read or write address generating circuit conforming to a predetermined logic of said fourth memory circuit and corner turners for permutating data read out from said fourth memory circuit.

4. A Fourier transform apparatus set forth in claim 1,

characterized in that in the case where the number a of said pipeline FFT circuits incorporated in the transform means of said preceding stage and said succeeding stage is two,

said first data supply means is comprised of fourth and fifth data permutating modules in two stages, said fourth and fifth data permutating modules being composed of fifth and sixth memory circuits for storing data, respectively, read or write address generating circuits conforming to predetermined logics of said fifth and sixth memory circuits, respectively, and corner turners for permutating data read out from said fifth memory circuit, and

that said second data supply means is comprised of a sixth data permutating module, said sixth data permutating module being composed of a seventh memory circuit for storing data, a read or write address generating circuit conforming to a predetermined logic of said seventh memory circuit.

5. A Fourier transform apparatus set forth in claim 1,

characterized in that in the case where the number a of said pipeline FFT circuits incorporated in the transform means of said preceding stage and said succeeding stage is one,

said first data supply means is comprised of seventh and eighth data permutating modules, said seventh data permutating module being composed of an eighth memory circuit for storing data, a read or write address generating circuit which conforms to a predetermined logic of said eighth memory circuit and a parallel-in serial-out circuit for permutating the data read out from said eighth memory circuit, while said eighth data permutating module includes a ninth memory circuit constituted by two banks so that upon data storing, data are written in said two banks alternately M by M data whereas upon data reading, corresponding data of corresponding data sets each of M point data are simultaneously read out from said two banks, respectively, to constitute two parallel inputs of said pipeline FFT circuit and a read or write address generating circuit which operates in conformance to a predetermined logic of said ninth memory circuit, and

that said second data supply means is comprised of a tenth memory circuit constituted by two banks so that upon data storing, data are written in said two banks alternately on an M-by-M basis whereas upon data reading, corresponding data of corresponding data sets each of M point data are simultaneously read out from said two banks, respectively, to constitute two parallel inputs of said pipeline FFT circuit and a read or write address generating circuit which operates in conformance to a predetermined logic of said tenth memory circuit.

6. A Fourier transform apparatus characterized in that the Fourier transform apparatuses set forth in of claim 3 to 5 is disposed in parallel in a number equal to a power of "2", time-serial input data are allocated to said Fourier transform apparatuses, respectively, on an N-by-N basis, where N (= M x M) represents a maximum number of points for Fourier transform, and that said Fourier transform

apparatus includes data distributing/ permutating means for supplying sets of contiguous M point data on an a-by-a basis in two parallel columns in each set and hence in 2a parallel columns in total to said Fourier transform apparatuses, respectively.

7. A Fourier transform apparatus set forth in claim 6, characterized in that said data distributing/permutating means is composed of an eleventh memory circuit for storing data corresponding to the number of Fourier transform apparatuses disposed in parallel, a read or write address generating circuit which conforms to a predetermined logic of said eleventh memory circuit and corner turners for permutating data read out from said eleventh memory circuit to output the data in parallel to said Fourier transform apparatuses, respectively, which are disposed in parallel.

8. A Fourier transform apparatus set forth in claim 1,

characterized in that said Fourier transform apparatus includes bypass means for bypassing arithmetic operation performed by the transform means of said preceding stage and said succeeding stage.